Sri Sri Sri Mookambika Educational Society's
VAAGDEVI INSTITUTE OF TECHNOLOGY & SCIENCE
Peddasettipalli (V), Proddatur - 516360
(Approved by A.I.C.T.E., New Delhi, Affiliated to JNTUA, Anantapuram)

Display of Internal Marks

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PEDDASETTIPALLI.
PRODDATUR. Kadapa (Dist.)

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Peddasettipalli (V), Proddatur-516360.

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I Mid Examination [Subjective Paper]

Year / Semester	:	III/II	Branch / Section	:	E.C. E
Course code / Title	:	20A04602T/ VLSI DESIGN	Date/Session	:	12/03/2024/FN
Total Marks	:	30	Duration	:	90 Minutes

COURSE OUTCOMES:

CO1	Acquire qualitative knowledge about the fabrication process of integrated circuit using MOS transistors	CO4	Design simple memories using MOS transistors and can understand design of large memories
CO2	Draw the layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	CO5	Understand the concept of testing and adding extra hardware to improve testability of system
CO3	Design building blocks of data path using gates.	CO6	

Answer all the Questions (3X10=30 Marks)

Q.No.		Question	CO	MARKS
1.	a.	What is Moore's law? State various IC technologies on the basis of number of transistors on a chip	CO1	2
	b.	What is the figure of merit of a MOS transistor? Mention the suitable expression for figure of merit	CO1	2
	c.	Explain in detail about the steps involved in CMOS IC fabrication process with essential diagrams.	CO1	6
		OR		
2.	a.	Describe the different operating regions for an MOS transistor	CO1	2
	b.	MOSFETs are said to be more efficient than BJTs. Justify the answer	CO1	2
	c.	Draw the Ids-Vds relationship curve and discuss in detail about its role in the MOS design equations	CO1	6
3.	a.	Define threshold voltage with suitable equation of a MOS device	CO2	2
	b.	Draw CMOS inverter.	CO2	2
	c.	Explain working of nMOS inverter	CO2	6
		OR		
4.	a.	What are limitations of scaling	CO2	2
	b.	Explain working of pass transistor logic	CO2	2
	c.	Design stick and layout diagram for CMOS inverter and 2 input NMOS gate	CO2	6
5.	a.	What is the importance of CMOS design rules	CO1	2
	b.	Define gate capacitance	CO1	2
	c.	Briefly discuss about scaling of MOS circuits and its limitations	CO1	6
		OR		
6.	a.	What do you mean by inverter delay? Explain	CO2	2
	b.	What are scaling models	CO2	2
	c.	Explain stick diagram rules	CO2	6

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Mr. S M K SUKUMAR REDDY/Assistant Professor/Dept. of E.C. E

HoD

Name : B. Lakshmi Prasanna
Roll No : 21L21A0446
class : III-year ECE
Section: B
subject : VLSI

5/5

Assignment-1

1. Explain in detail about the steps involved in cmos Ic fabrication process with essential diagrams.

CMOS fabrication can be accomplished using either of the three technology.

- N-well technologies (P-well technologies
- Twin well technology.
- silicon on insulator (SOI)

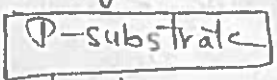
The fabrication of CMOS can be done by using following the below shown twenty steps, by which cmos can be obtained by Integrating both the NMOS and PMOS transistors on the same chip substrate for Integrating these NMOS and PMOS devices on the same chip. Special regions called as well or tubs are required in which semiconductor type and substrate type are opposite to each other. A P-well has be created on a N-substrate or N-well has to be created on a P-substrate. In this article, the fabrication of CMOS is described using the P-substrate. In which the NMOS-transistor is fabricated on a P-type substrate and the PMOS transistor is fabricated in N-well.

The fabrication process involves twenty steps. which one as follows.

N-well process

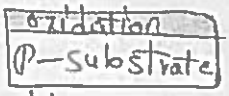
step-1:- substrate

The primarily. start the process with a P-substrate.



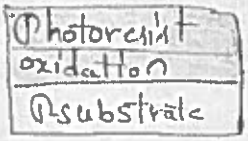
step2:- oxidation

The oxidation process is above done by using high purity oxygen and hydrogen, which are exposed in a oxidation furnance approximately at 1000 degree centigrade.



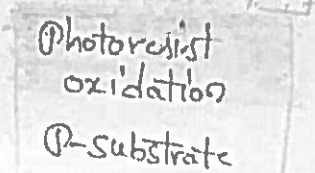
step3:- Photoresist

A light-sensitive polymer that software softens whenever exposed to light is called as photoresist layer it is formed.



step4:- Masking

The Photoresist is exposed in uv rays through the N-well Mask.



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2	2	L	2	5	A	0	4	D	9

I Mid Examination [Objective Paper]

Year / Semester	:	III II	Branch / Section	:	ECE
Course code / Title	:	20A04602T VLSI DESIGN	Date/Session	:	12/03/2024/EN
Total Marks	:	10	Duration	:	20 Minutes

Answer all the questions (20 X 0.5 marks = 10 Marks)

Q. No.	Question				Answer Choice	CO
1.	VLSI technology uses to form integrated circuit using				A	CO1
	A. Transistors	B. Switches	C. Diodes	D. buffers		
2.	Medium scale integration has				C	CO1
	A. 10 logic gates	B. 50 logic gates	C. 100 logic gates	D. 1000 logic gates		
3.	nMOS fabrication process is carried out in				A	CO1
	A. thin wafer of a single crystal	B. thin wafer of multiple crystals	C. thick wafer of a single crystal	D. thick wafer of multiple crystals		
4.	Contact cuts are made in				A	CO1
	A. Source	B. Drain	C. Metal layer	D. Diffusion layer		
5.	CMOS technology is used in developing				D	CO1
	A. Microprocessors	B. Microcontrollers	digital logic circuits	D. All		
6.	Which type of CMOS circuits are good and better?				B	CO2
	A. P well	B. N well	C. Both a and b	D. None		
7.	What are the advantages of BiCMOS?				D	CO2
	A. higher gain	B. high frequency characteristics	C. better noise characteristics	D. all		
8.	What are the features of BiCMOS?				A	CO2
	A. low input impedance	B. high packing density	C. high input impedance	D. bidirectional		
9.	Which has high input resistance?				C	CO2
	A. NMOS	B. BMOS	C. BiCMOS	D. None		
10.	Ids depends on				B	CO2
	A. Vg	B. Vds	C. Vdd	D. Vss		
11.	Stick diagrams are those which convey layer information through				B	CO3
	A. Thickness	B. Colour	C. Shapes	D. layers		
12.	Design rules does not specify				D	CO4
	A. Line widths	B. Separations	C. Extensions	D. colours		
13.	Which gives scalable design rules?				A	CO4
	A. Lambda rules	B. Micron rules	C. Layer rulers	D. Thickness rules		
14.	act as a interface in between actual layout and symbolic circuits				C	CO3
	A. Pie diagram	B. vean diagram	C. stick diagram	D. both a and b		
15.	What are different regions in which MOS transistor operate				D	CO3
	A. Cutoff region	B. Saturation region	C. Non-saturated region	D. all		
16.	Pull up devices can drag the voltage at output to				B	CO3
	A. Zero volts	B. Upper supply voltage	C. Lower supply voltage	D. none		
17.	Green color in the stick diagram represents				A	CO3
	A. N-diffusion	B. P-diffusion	C. Polysilicon	D. None		
	[illegible] commonly used scaling models				C	CO3
	[illegible]	B. Constant voltage	C. Both a and b	D. None		
	[illegible] size and to achieve higher packing density of circuitry on chip				A	CO3
	[illegible]	B. Fading	C. Expansion	D. None		
	[illegible] mode, device is in [illegible] conditon				A	CO3
	A. Conducting	B. Non conducting	C. Partially conducting	D. none		

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Mr S M K Sukumar Reddy
Assistant Professor/ E.C.E

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INTERNAL EXAMINATION MAIN ANSWER BOOK

Mid Examination	I	II	III	I
Name	S.Neelima			
H.T.No.	21L81A0473			
Class & Branch	III ECE-B			
Subject	VLSID			
Sign of Student	S.Neelima			
Sign of invigilator with Date				

Q.No.	a	b	c	Total
1	2	2	6	10
2				
3				
4	2	2	6	10
5				
6	2	2	6	10
Grand Total Marks				30/30

15/15

1a) Moore's law:

The transistors on an Integrated circuit will be double at every 18 months.
This is observed by Moore in Emroutes of Intel corporation

→ Various Ic technologies on the basis of no. of transistors on a chip.

* Small scale integration → 1 - 100 transistor on chip
* Medium scale integration → 100 - 1000 transistors
* Large scale integration → 1000 - 10000 transistors
* Very Large scale integration → 10000 - 1 Million transistor
* Ultra Large scale integration → 1 Million - 10 Million
* Giant scale integration → above 10 million transistors

2

1b) Figure of Merit:

$$\text{Figure of merit} = \frac{\mu C_g}{L^2}(V_{gs} - V_t)$$

The figure of merit depends on gate capacitance, threshold voltage above gate voltage, carrier mobility and inversely proportional to the square of the channel length.
If the figure of merit is high, the transistor works with high input impedence.
i.e., $\mu_n > \mu_p$ which results in nMOS transistors work faster than PMOS transistors.

2

B. Siddappa

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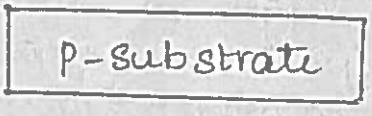
(c) CMOS IC fabrication:

The fabrication of CMOS involves 20 steps. CMOS is the combination of both pMOS and NMOS. CMOS involves in 3 fabracation techniques

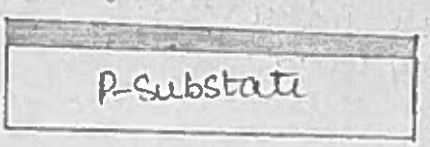
* N-well
* P-well
* Silicon substrate

The most commonly used is N-well fabrication technique. In N-well fabrication the p-substrate with N-diffusion form N-well whereas N substrate with p diffusion form P-well.

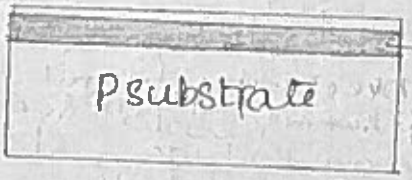
Step1: Substrate: consider the p-substrate



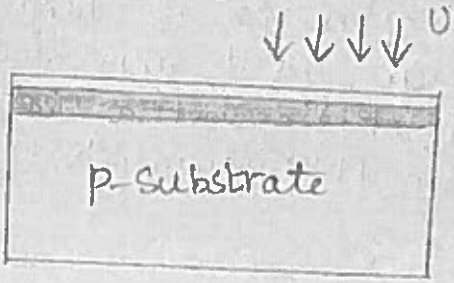
Step2: oxidation: Oxidation of psubstrate with O_2 and H_2.



Step3: photoresist: It is the layer when exposed to Light rays to get layer.



Step4: The psubstrate is exposed to UV rays in order to form N-well



B. Siddeswara

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ADDITIONAL ANSWER BOOK

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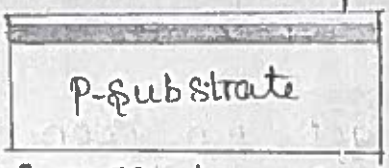
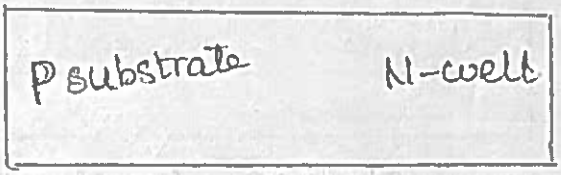
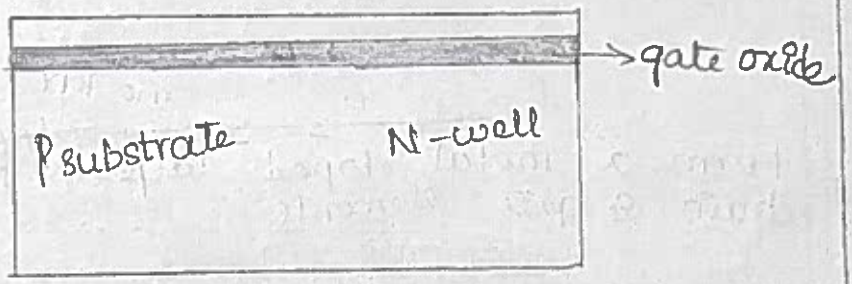
Step 5: Masking
Masking involves a layer of to be removed with the masking.



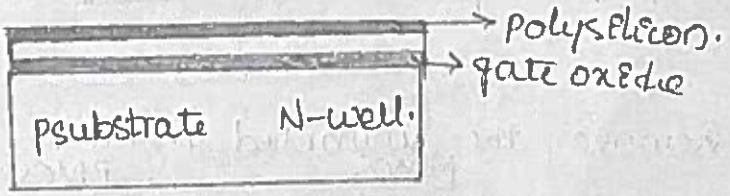
Step 6: Etching is done to remove unwanted material in the p-substrate to form N-well.



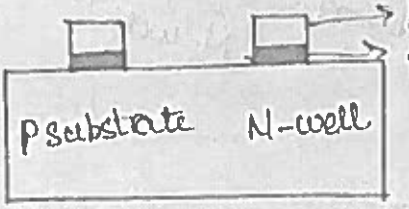
Step 7: A oxidation is formed to form the gate oxide layer on the psubstrate and N-well layer



Step 8: Form a polysilicon layer to get the gate elements.



Step 9: Removal of unwanted material to get the gate layers



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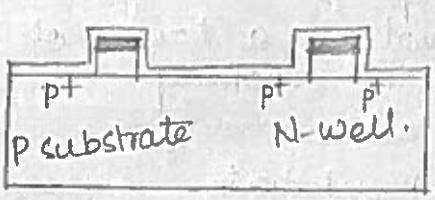
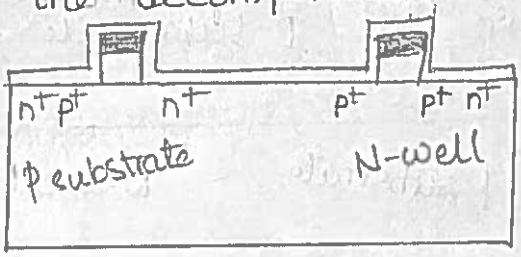
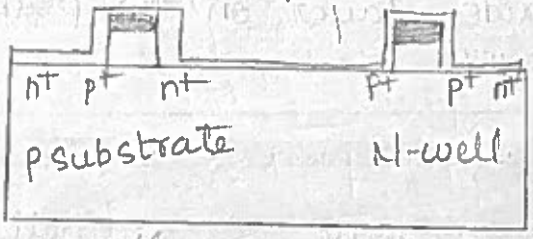
Step 10: Form a diffusion layer to get the using chemical vapour decomposition to get ion layers for the p^+ ions.



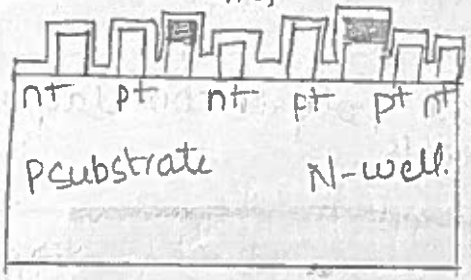
Similarly to get n ion on the wafer by the decomposition.



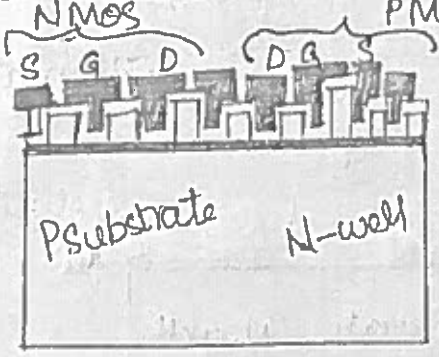
Removal of oxidation layer to form source, drain and gate elements



Form a metal doped layers for the drain & gate elements



Remove the unwanted metal.



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ADDITIONAL ANSWER BOOK

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4a) Limitation of scaling:

Scaling means to reduce feature size and to achieve high packing density of circuitary on chip.
This results in minaturization which can decrease the area and the scaling factor.
Three categories of minaturization involves in scaling

2

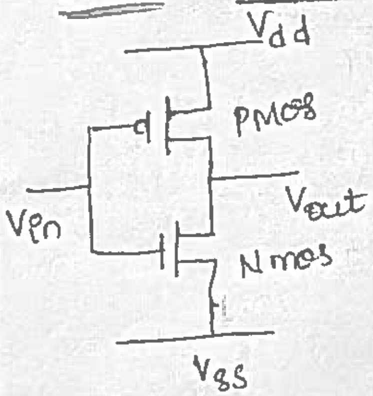
4b) Pass transistor logic:

Unlike biploar transister, the gate capacitance is independent of the voltage which involves in passing transistor logic. which allows voltage in the transistor.

2

4c) CMOS Inverter:

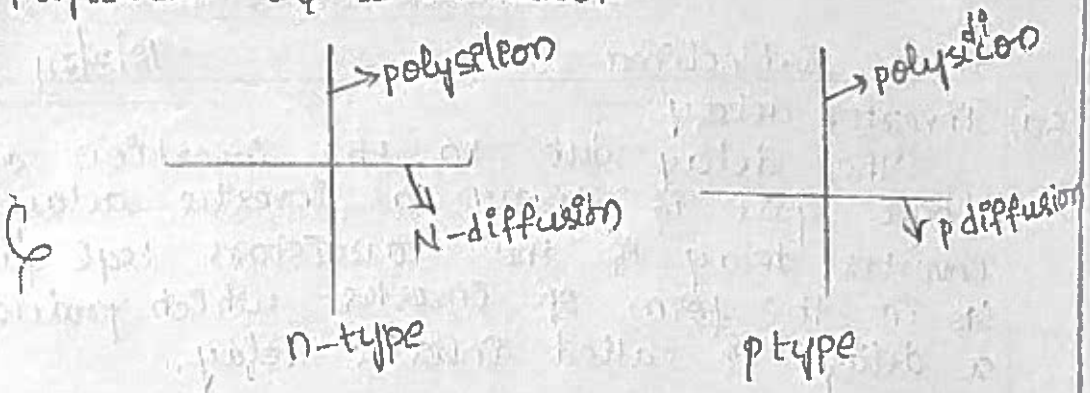
Circuit diagram:



For the CMOS inverter, we know the CMOS is a combination of both nMOS and PMOS transistor. For the single i/p CMOS inverter requires one PMOS and 1nMOS transistor in the series connection

* The stick diagram of CMOS inverter is Vdd and and are coloured with blue
* When a diffusion is cross over with polysilicon forms a transistor.

Rule 3: When a diffusion cross over with polysilicon forms a transistor.



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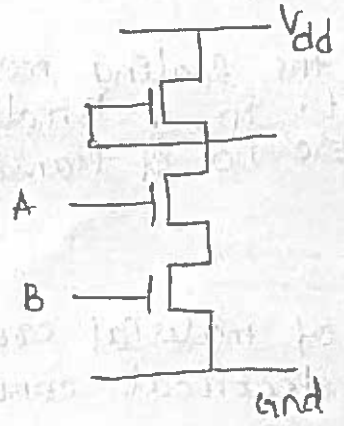
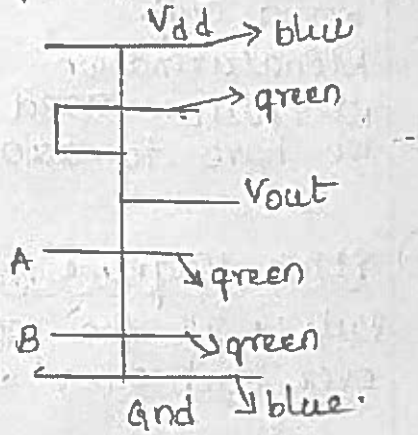
(4C) 2 input NMOS inverter

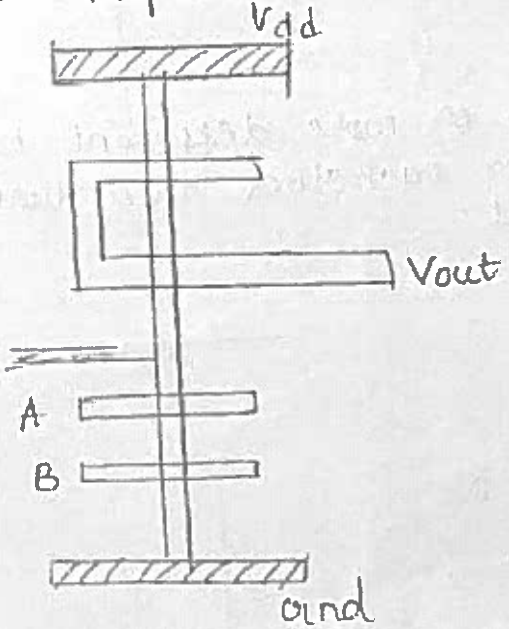
circuit diagram



stick ~~layout~~ diagram



layout diagram



6

A. Siddesh
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6a) Inverter delay:

The delay due to the invertion of logic gate is known as Inverter delay. Inverter delay is the transistors logic gates one in the form of Inverter which produces a delay is called Inverter delay.

6b) Scaling models:

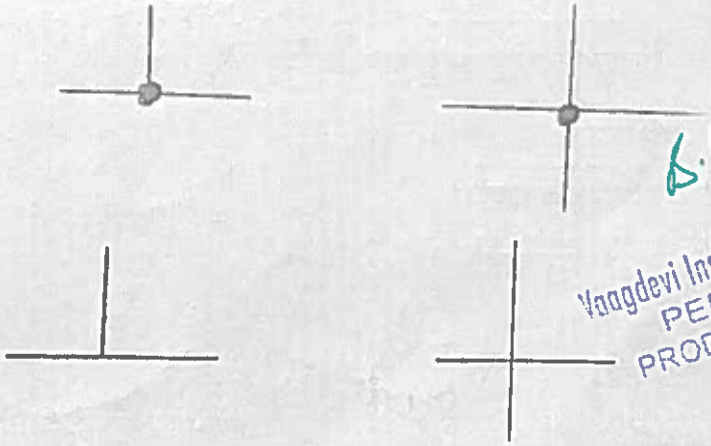
Scaling means to reduce feature size and produce high packaging density of circuitary on a chip.

Miniaturization is one of the scaling model. To reduce area and cost. In a small area we have to accomodate more no. of transistors.

6c) Stick diagrams rules:

Rule 1: If the same type of material cross over each other form an electrical contact.

Rule 2: When two or more different type of material cross over each other then there is no electric contact.



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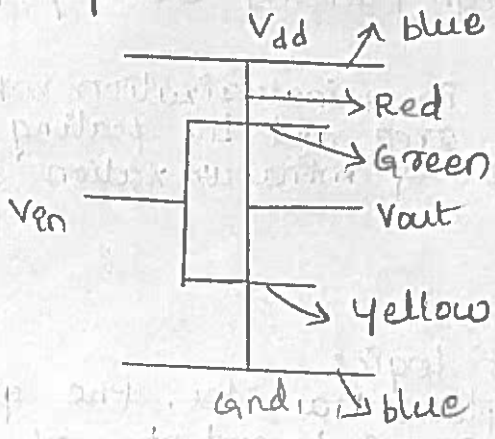
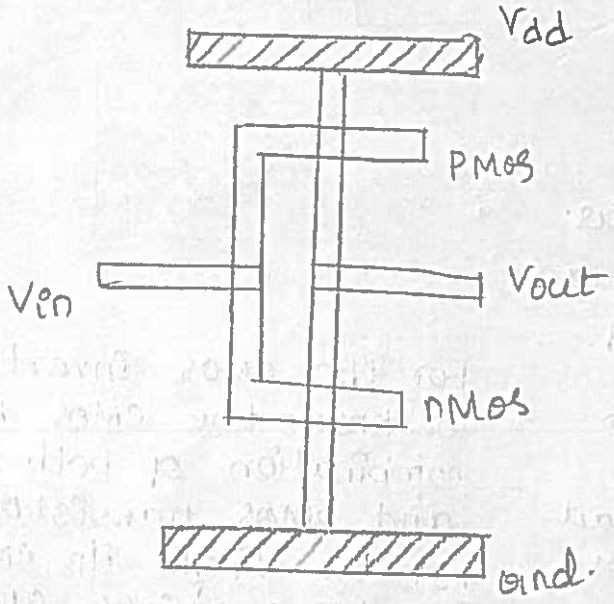
If diffusion is N type nMOS transistor
If diffusion is P type PMOS transistor
polysilicon is in red colour.
P-diffusion is in green colour.
N-diffusion is in yellow colour

Stick diagram:



Layout diagram:



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Peddasettypalli(V), Proddatur.

B.Tech I Year I Semester (R23) Internal Marks

Branch: CSE | **College Code:L2**

Academic Year: 2023-24

	1-(23A52201T) Communicative English	10-(23A99201) Health and Wellness, Yoga and Sports	2-(23A51202T) Chemistry	3-(23A54101) Linear Algebra & Calculus	4-(23A01201T) Basic Civil & Mechanical Engineering	5-(23A0501T) Introduction to Programming	6-(23A52201P) Communicative English Lab	7-(23A51202P) Chemistry Lab	8-(23A03201) Engineering Workshop	9-(23A05101P) Computer Programming Lab	Grand Total
23L21A0501	29	30	28	28	27	25	27	27	29	29	279
23L21A0502	26	30	24	27	22	22	26	25	27	26	255
23L21A0503	20	30	16	24	20	16	22	22	22	20	212
23L21A0504	24	30	20	23	22	17	23	23	23	24	229
23L21A0505	28	30	27	23	24	18	26	26	27	25	254
23L21A0506	25	30	27	27	25	22	27	27	26	27	263
23L21A0507	22	30	24	23	23	18	22	22	22	20	226
23L21A0508	19	30	24	21	22	19	24	24	23	20	226
23L21A0509	29	30	29	30	26	28	27	28	29	29	285
23L21A0510	28	30	25	27	24	22	30	27	28	28	269
23L21A0511	29	30	30	29	27	26	30	27	29	30	287
23L21A0512	29	30	30	28	27	29	28	30	27	30	288
23L21A0513	23	30	20	17	20	15	22	23	22	20	212
23L21A0514	28	30	28	27	29	24	29	29	27	29	280
23L21A0515	29	30	29	27	29	29	28	29	29	30	289
23L21A0516	27	30	27	24	26	24	27	27	28	28	268
23L21A0517	30	30	30	30	29	26	28	29	29	29	290
23L21A0518	26	30	24	20	20	17	24	25	25	25	236
23L21A0519	24	30	25	23	20	15	23	22	22	22	226
23L21A0520	28	30	30	28	25	27	26	28	28	28	278
23L21A0521	27	30	27	27	25	25	26	25	26	28	266
23L21A0522	18	30	15	18	16	15	22	22	24	24	204

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B.Tech I Year I Semester (R23) Internal Marks

Branch: CSE | **College Code:L2**

Academic Year: 2023-24

	1-(23A52201T) Communicative English	10-(23A99201) Health and Wellness, Yoga and Sports	2-(23A51202T) Chemistry	3-(23A54101) Linear Algebra & Calculus	4-(23A01201T) Basic Civil & Mechanical Engineering	5-(23A0501IT) Introduction to Programming	6-(23A52011P) Communicative English Lab	7-(23A51202P) Chemistry Lab	8-(23A03201) Engineering Workshop	9-(23A05101P) Computer Programming Lab	Grand Total
23L21A0523	24	30	24	23	19	20	25	25	25	28	243
23L21A0524	27	30	28	26	23	20	27	26	27	27	261
23L21A0525	30	30	30	30	29	30	30	30	30	30	299
23L21A0526	25	30	26	28	20	19	25	25	25	25	248
23L21A0527	24	30	24	27	23	22	26	24	25	25	250
23L21A0528	29	30	30	30	29	26	29	30	30	29	292
23L21A0529	30	30	29	27	27	22	28	28	28	28	277
23L21A0530	28	30	29	30	27	23	27	26	29	29	278
23L21A0531	27	30	26	26	24	21	27	25	28	28	262
23L21A0532	22	30	23	23	22	21	26	26	27	27	247
23L21A0533	21	30	24	23	23	19	23	22	22	22	229
23L21A0534	23	30	26	26	24	19	26	24	27	27	252
23L21A0535	22	30	26	26	22	25	28	26	24	27	256
23L21A0536	21	30	23	23	19	22	23	23	22	25	231
23L21A0537	25	30	26	24	21	15	23	22	22	24	232
23L21A0538	27	30	29	23	25	20	29	28	26	28	265
23L21A0539	28	30	29	28	26	26	29	28	29	29	282
23L21A0540	29	30	29	30	29	24	29	29	29	28	286
23L21A0541	29	30	29	30	26	25	28	28	29	28	282
23L21A0542	22	30	25	27	18	15	23	22	25	25	232
23L21A0543	28	30	29	26	26	21	28	27	27	27	269
23L21A0544	20	30	20	20	17	15	23	23	22	20	210

A. Sahitya M. Lakshmi Devi K. V. Prabhakar Reddy A. Sahitya M. Lakshmi Devi T. V. Reddy T. V. Reddy

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B.Tech I Year I Semester (R23) Internal Marks

Branch: CSE | **College Code:L2**

Academic Year: 2023-24

	1-(23A52201T) Communicative English	10-(23A99201) Health and Wellness, Yoga and Sports	2-(23A51202T) Chemistry	3-(23A54101) Linear Algebra & Calculus	4-(23A01201T) Basic Civil & Mechanical Engineering	5-(23A0501IT) Introduction to Programming	6-(23A52201P) Communicative English Lab	7-(23A51202P) Chemistry Lab	8-(23A03201) Engineering Workshop	9-(23A05101P) Computer Programming Lab	Grand Total
23L21A0545	25	30	22	21	23	21	29	24	28	27	250
23L21A0546	20	30	26	19	20	17	26	23	26	26	233
23L21A0547	30	30	28	29	23	26	30	26	27	29	278
23L21A0548	23	30	22	23	22	17	26	25	25	25	238
23L21A0549	24	30	22	23	24	24	25	26	26	26	250
23L21A0550	22	30	23	23	26	20	27	23	24	24	242
23L21A0551	21	30	19	21	19	17	23	23	25	25	223
23L21A0552	30	30	29	28	29	25	30	29	30	30	290
23L21A0553	28	30	30	29	24	25	27	26	24	28	271
23L21A0554	25	30	24	27	21	19	25	23	22	24	240
23L21A0555	26	30	29	29	23	22	26	26	27	29	267
23L21A0556	24	30	24	25	21	27	28	24	24	28	255
23L21A0557	21	30	22	25	18	15	28	26	25	26	236
23L21A0558	30	30	29	28	27	23	30	30	30	30	287
23L21A0559	26	30	29	30	23	23	30	28	27	29	275
23L21A0560	30	30	30	30	27	25	30	30	30	30	292
23L21A0561	24	30	23	24	21	17	24	23	22	24	232
23L21A0562	30	30	30	29	30	29	30	30	30	30	298
23L21A0563	25	30	24	20	19	20	29	24	22	26	239
23L21A0564	29	30	30	30	28	28	26	28	27	27	283
23L21A0565	30	30	29	27	26	27	27	27	29	30	282
23L21A0566	27	30	27	27	26	24	26	28	27	28	270

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B.Tech I Year I Semester (R23) Internal Marks

Branch: ECE | **College Code:L2**

Academic Year: 2023-24

	1-(23A56101T) Engineering Physics	10-(23A99101) NSS/NCC/Scouts & Guides/ Commun	2-(23A54101) Linear Algebra & Calculus	3-(23A02101T) Basic Electrical & Electronics	4-(23A03101T) Engineering Graphics	5-(23A05101T) Introduction to Programming	6-(23A05102) IT Workshop	7-(23A56101P) Engineering Physics Lab	8-(23A02101P) Electrical & Electronics Engineer	9-(23A05101P) Computer Programming Lab	Grand Total
23L21A0401	29	30	26	29	30	25	30	30	28	29	286
23L21A0402	29	30	29	30	30	30	30	30	30	29	297
23L21A0403	18	30	15	16	23	17	25	24	26	26	220
23L21A0404	16	30	19	27	27	18	26	25	25	27	240
23L21A0405	25	30	21	26	28	22	29	28	29	26	264
23L21A0406	26	30	25	29	29	24	25	29	25	29	271
23L21A0407	30	30	27	29	30	30	30	30	30	30	296
23L21A0408	16	30	20	20	25	19	27	24	25	22	228
23L21A0409	26	30	18	25	28	26	28	29	28	28	266
23L21A0410	27	30	23	28	30	28	29	29	29	28	281
23L21A0411	17	30	18	24	26	20	27	25	27	20	234
23L21A0412	21	30	16	24	27	19	27	25	27	24	240
23L21A0413	22	30	20	29	27	23	25	26	25	29	256
23L21A0414	22	30	16	25	28	20	29	28	28	25	251
23L21A0415	23	30	22	28	28	21	28	28	28	28	264
23L21A0416	25	30	20	28	30	24	29	28	29	28	271
23L21A0417	30	30	30	29	30	30	30	30	30	30	299
23L21A0418	18	30	19	27	28	22	27	26	27	27	251
23L21A0419	23	30	24	27	30	24	28	27	28	26	267
23L21A0420	24	30	21	28	29	29	29	27	29	29	275
23L21A0421	18	30	18	23	24	21	25	24	25	20	228
23L21A0422	21	30	19	24	29	20	28	29	30	20	250
23L21A0423	26	30	27	28	30	26	29	29	28	28	281
23L21A0424	24	30	20	28	28	20	27	27	27	28	259
23L21A0425	29	30	29	29	30	30	30	30	30	30	297

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B.Tech I Year I Semester (R23) Internal Marks

Branch: EEE | **College Code:L2**

Academic Year: 2023-24

	1-(23A52201T) Communicative English	10-(23A99201) Health and Wellness, Yoga and Sports	2-(23A51202T) Chemistry	3-(23A54101) Linear Algebra & Calculus	4-(23A01201T) Basic Civil & Mechanical Engineerin	5-(23A05101T) Introduction to Programming	6-(23A52201P) Communicative English Lab	7-(23A51202P) Chemistry Lab	8-(23A03201) Engineering Workshop	9-(23A05101P) Computer Programming Lab	Grand Total
23L21A0201	24	30	25	22	25	22	27	26	27	28	256

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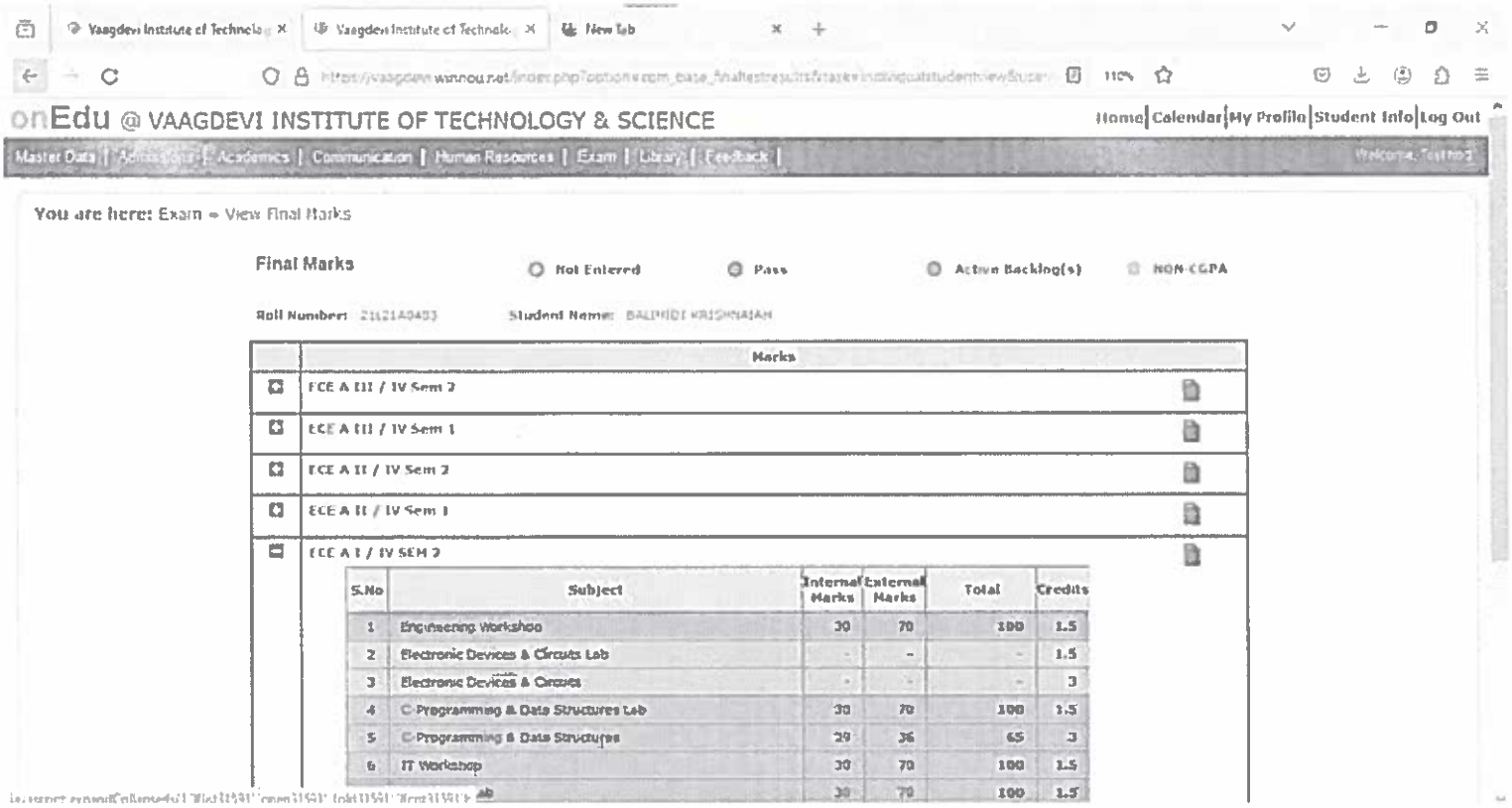

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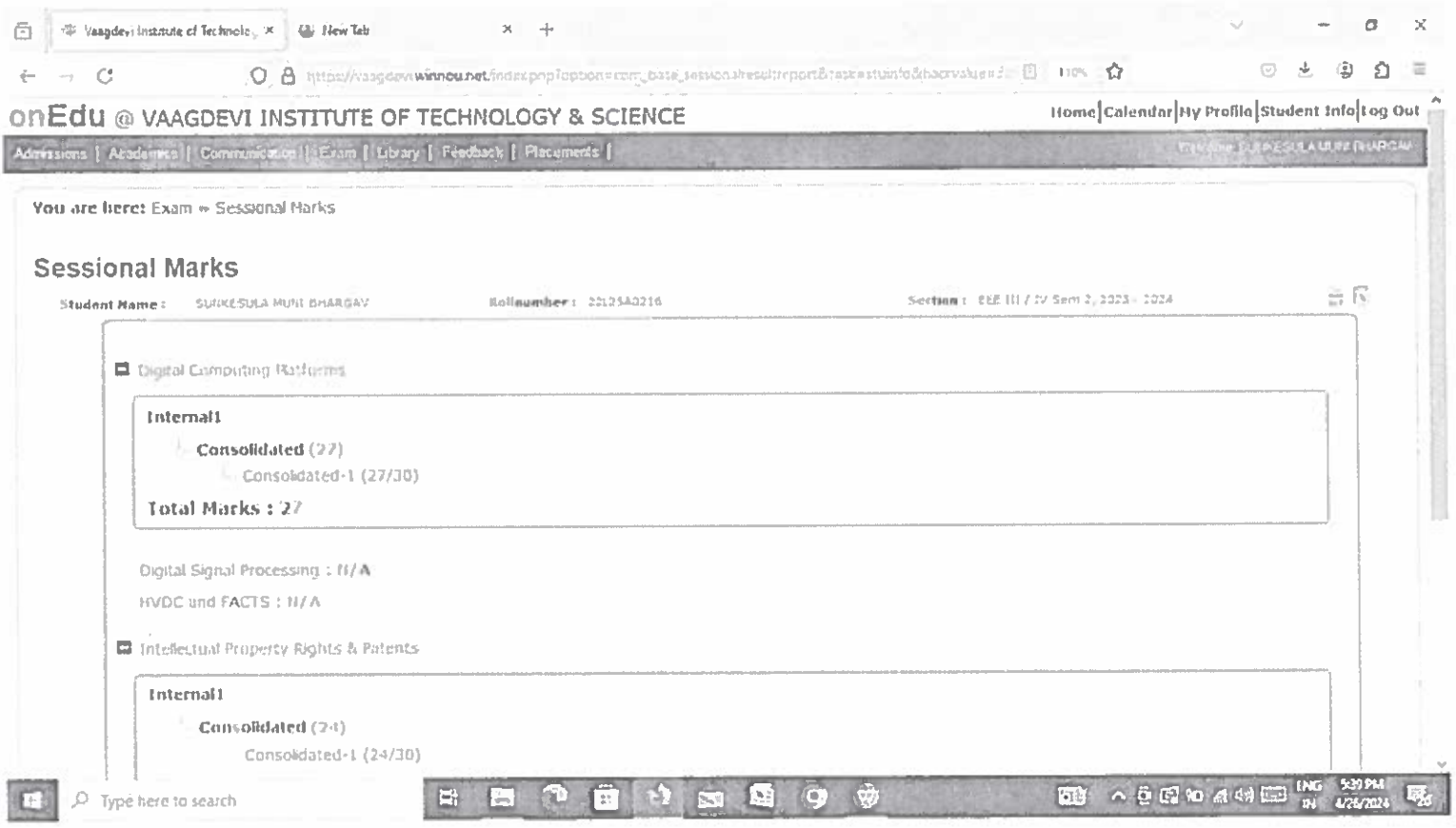

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